REMARKS

This is in response to the Office Action of February 6, 2004 in which the Examiner rejected claims 25-44. Claim 25-44 are pending.

Claims 25-27 and 37 were rejected under 35 U.S.C 103(a) over Fujimoto (U.S. Pat. No. 5,559,952). Claims 28-29 and 38-44 were rejected under 35 U.S.C. 103(a) over Fujimoto in view of Wada (U.S. Pat. No. 5,959,639). Claims 30-36 were rejected under 35 U.S.C. 103(a) over Fujimoto in view of Wada and Holt (U.S. Pat. No. 5,760,792). Claims 34 and 35 were rejected under 35 U.S.C. 103(a) over Fujimoto in view of Wada and Holt and further in view of Porterfield (U.S. Pat. No. 6,069,638).

Fujimoto is utilized as the basis for all of the claim rejections. The Examiner contends in section two of the Office Action that: "it would have been obvious to one of ordinary skill in the art at the time the present invention was made that the cache memory of Fujimoto can be used to store any information, such as graphics/image data (texture, depth, color, vertex, pixel data), instruction, or commands because that is what a cache memory for." The Examiner also appears to contend that it would therefore be obvious to use the frame buffer cache of Fujimoto to cache vertex data for use in rendering.

Applicant respectfully traverses the rejections. The Examiner is not considering Fujimoto as a whole, which provides no teaching or suggestion for modifying its frame buffer cache in the manner indicated by the Examiner. Moreover, the Examiner is engaging in impermissible hindsight based on Applicant's disclosure.

Fujimoto does not disclose an arbitrary cache but a frame buffer cache 141 dedicated to storing the same type of image data as that stored in a dual port image memory Video Random Access Memory (VRAM) 30, as described in column 5, lines 55-59. The frame buffer cache 141 "holds part of image data stored in the dual port image memory (VRAM) 30," as described in column 5, lines 58-59.

Additionally, frame buffer cache 141 has a specific function, namely it is a cache configured to permit simultaneous read/write operations of image data in frame buffer cache 141 and VRAM 30. Image data is periodically transferred between VRAM 30 and frame buffer cache 141, as described in column 7, line 65 to column 8, line 3. When requested image data is in frame buffer cache 141, the image data is read out from the frame buffer cache, eliminating

the need for a read access to be performed on VRAM 30 for the requested data, as described in column 5, lines 60-64. The benefit of a dedicated frame buffer cache is that it eliminates a wait state by permitting the CPU or the drawing coprocessor to perform an image data read/write operation simultaneously with an access operation of the VRAM 30, as described in column 9, lines 34-39.

The image data stored in the VRAM (and hence in its cache, frame buffer cache 141) corresponds to data that may be displayed on a screen, such as pixel data and text data, as described in column 4, lines 46-67. This can also be observed in the circuit of Figure 1. Fujimoto states that the portion of the circuit below VRAM 30 (e.g., serializer 20, color palette controller 24, sprite controller 27, etc.) "constitute a display circuit for displaying image data stored in the dual port image memory (VRAM) 30, on the flat panel display 40 of the color CRT display 50," as described in column 6, lines 18-25.

Applicant also notes that it is well understood in the art that the type of image data stored in a VRAM (and hence in a corresponding VRAM cache) corresponds to the image to be displayed, i.e., pixel data and text data. Applicant has attached Exhibits 1-4, which describe common definitions of a Video Random Access Memory (VRAM) to demonstrate that one of ordinary skill in the art would understand that VRAM 30 (and hence frame buffer cache 141) stores image data to be displayed on a CRT display, where the image data corresponds to pixel data and text data.

Applicant also notes that Fujimoto does not provide a teaching or suggestion for a display controller that renders locally cached vertex data. No such function is described in Fujimoto. On the contrary, the frame buffer cache 141 of Fujimoto is dedicated to a completely different function, namely eliminating a wait state by caching VRAM data to permit read/write operations of VRAM data in a frame buffer cache 141 while also permitting simultaneous access to a VRAM 30.

In light of the above discussion, Applicant respectfully submits that Fujimoto does not provide a teaching or suggestion for a cache that stores vertex data for rendering pixels. Vertex data is not image data that can be displayed on a screen as defined by Fujimoto or in accordance with common definition of the type of image data stored in a VRAM. Moreover, Fujimoto does not teach or suggest using locally cached vertex data to render pixels.

In regards to Wada, Applicant notes that the video cache 10 of Wada is also a cache for frame data, i.e., pixel data. There is no teaching or suggestion in Wada for a memory transfer of vertex data to a vertex cache.

The Examiner also appears to be engaging in impermissible hindsight in light of Applicant's disclosure. None of the references cited by the Examiner recognize the problem that Applicant's claimed invention is directed towards. Applicant's specification describes the benefits of caching vertex data in a graphics module to reduce the amount of data that a CPU must transfer over a system bus to a graphics module. In a system in which a graphics module renders pixels based on vertex data sent by a CPU over a system bus, caching vertex data in the graphics module reduces the amount of data that must be transferred by the CPU over the system bus. In the embodiment described in claims 27, 30, 37, and 41 the data transfer requirements are further reduced by using index values for cache entries, i.e., a CPU needs only to send the index values of vertices that are cached. In the embodiments of claims 30, 38, and 41, the data transfer burden on the CPU is further reduced by having the graphics module perform a direct memory transfer for missing vertex data.

Consequently, in view of the foregoing amendments and remarks, it is respectfully submitted that all pending claims in the application are now in a condition for allowance. The Examiner is invited to contact the undersigned if there are any residual issues that can be resolved through a telephone call.

The Commissioner is hereby authorized to charge any appropriate fees to Deposit Account No 03-3117.

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Respectfully submitted,
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